REMARKS

Claims 1-11 and 13-33 are currently pending in this application. Claims 18-22 have been allowed. Claims 2, 4, 7, 11, 12 and 15 were objected to as being dependent upon a rejected base claim, but the Examiner has indicated that they would be allowable if rewritten in independent form, including parent limitations. Claim 12 is cancelled by way of this amendment. Claims 23-33 have been added. Claims 1, 3, 5, 6, 8-10, 13, 14, 16 and 17 stand rejected under 35 U.S.C. §103. Reconsideration and further examination of the rejected claims is respectfully requested for the reasons provided below.

Rejections under 35 U.S.C. §103

Claims 1, 3, 5, 6, 8-10, 13, 14, 16 and 17 were rejected under 35 U.S.C. §103 as being unpatentable over Hershey et al (U.S. Patent 6,167,062) in view of Miller (U.S. 5,930,231).

Hershey, U.S. Patent 6,167,062

Hershey addresses the problems of payload mapping, stating "The essence of the payload mapping process is to synchronize the tributary signal with the envelope capacity provided for transport. This is achieved by adding extra stuffing bits (also called justification bits) to the STS-1 signal bit stream as part of the mapping process. For example, a DS3 tributary signal at a nominal rate of 44 Mbps needs to be synchronized with an envelope capacity of 51.840 Mbps (minus STS path overhead). In such manner an, asynchronous low bandwidth payload is embedded within a high bandwidth multiplexed synchronous signal..." (Col. 1 lines 38-53). Hershey states that before Hershey's invention "it was not easy to reliably retrieve the

asynchronous timing relationships between individual payloads subsequent to the signal processing function..."

Hershey describes "... System modules are provided for connection to a telecommunications network. The modules demultiplex asynchronous payloads, synchronize them, process them, and then restore their asynchronous relationships..." (col. 2, lines 9-13). At column 4. lines 62-68 through column 5, lines 2, Hershey describes:

"... The control and management memory and circuitry module 130a includes programmable hardware such as Field Programmable Gate Arrays (FPGA) which permit dynamic configuration of the network interface section 30 in accordance with network performance parameters, or though operator supplied modifications. In this way, the architecture of the network interface board is not limited by either the network protocol or the physical connection, but is reconfigurable through the control and management memory and circuitry..."

Miller, U.S. Patent 5,930,231

Miller describes a system for coupling telephony or other signals to a broadband network such as a CATV network. The system includes a block receiver that receives a group of modulated telephony signals communicated in a predetermined spectral subband selected within the upstream signal path in a broadband communication system, and provides individual modulated digital telephony signal outputs that are coupled to the telephony network. (col. 7, likes 10-16).

The Office Action states, at pages 2-3, in part:

"... Hershey discloses synchronization and control in a telecommunication system... Hershey is silent on transparent system with a receiver that extracts data signals and data clock. In analogous art, Miller discloses a spectrum receiver wherein (Abstract, col. 4, line 50-61) high data rate (SONET) information is received, receiver strips (col. 5, lines 37-50, col. 8, line 44-60) data from signal, extracting timing information (co. 13, line 16-26), (col. 26, line 37-47) FPGA provides frame synchronization, transmission is done in a transparent manner (Fig. 8, col. 13, line 1-36, col. 26, line 61-67 input/output interfaces (I/O ports), and it is inherent logic gates are

provided by FPGA. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have been motivated to implement a transparent system that includes a receiver that extracts data signals and timing information as taught by Miller with the teachings of Hershey for the purpose of mapping and synchronization in a high speed data rate system..."

To establish a *prima facie* case of obviousness under 35 U.S.C. §103, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Applicants submit that the rejection put forth in the Office Action does not meet this burden.

No motivation for the Modification suggested by the Examiner

It is well established that, in order to support a rejection under 35 U.S.C. §103, sufficient motivation for combining the references to reach the combined modification must be shown by the Examiner. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination *In re Mills, 916* F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Assuming that the references teach what the Examiner suggests, Applicant's submit that the motivation provided by the Examiner for this combination is insufficient. The Examiner has stated that Hershey would be motivated to extract the 'user signal and data clock' "for the purpose of mapping and synchronization in a high speed data rate system." However, Hershey *already* performs this function, and thus it cannot be seen by the Applicant how the gathering of this extra information

would serve to provide an advantage to Hershey. For at least the reason that this motivation is insufficient, the rejection under 35 U.S.C. §103 is insufficient and should be withdrawn.

However, even if the motivation is sufficient, Applicants submit that Hershey teaches away from such a limitation. A reading of Hershey seems to state that the received data is a combination of synchronous and asynchronous data, which has been combined using the payload packing approach, and thus is data having at least two clock frequencies. Hershey describes that "the SMC section 50 uses a 'fast clock' signal to synchronize the plurality of asynchronous payloads passed from the interface section 30 ... so that signal processing section 110 can operate in a synchronous mode on the payloads... The fast clock oscillator 62 generates a clock signal that is faster than the fastest payload clock of a set of payload clocks available through bus interface circuitry 52, thus ensuring that all payloads can be processed with the fast clock cycle..." Because Hershey teaches the benefits of 'a fast clock', Applicant's submit that the prior art teaches away from the desirability of the modification suggested by the Examiner, and that therefore the combination is improper and the rejection should be withdrawn.

Combination neither describes nor suggests the claimed invention

Claims 1, 3, 5, 6, 8 and 9:

Assuming that a motivation can be found and a combination can be properly made, Applicants submit that the combination still neither describes nor suggests the claimed invention. For example, Applicants claim 1 recites "...A transparent port for a high rate network comprising ... a receiver unit for receiving an incoming signal of an arbitrary data rate R1 and *extracting a user signal and a data clock* ... a programmable link termination PLT for reporting a set of performance parameters for said incoming signal; and a processing unit for recognizing a

plurality of provisioned protocols, selecting a first protocol characterizing said incoming signal and configuring said PLT according to said first protocol..." The Examiner admits that Hershey neither describes nor suggests the steps of "extracting a user signal and a data clock", but states that Miller discloses "... extracting timing information..." However, the portions of Miller that the Examiner indicates are discussions around TDM transmission, DMT transmission. Applicants respectfully submit that, while TDM may use time slots to retrieve information, and DMT may modulate carriers of certain frequencies with data, neither of these protocols 'extracts user signals and a data clock' as stated in claim 1. Accordingly, for at least this reason, claim 1 is patentably distinct over the combination of Miller and Hershey, and the rejection should be withdrawn.

Claims 3, 5, 6, 8 and 9 depend on claim 1, add further patentable limitations to claim 1, but are allowable for at least the reasons discussed with regard to claim 1.

Claims 10, 13, 14, 16 and 17

Applicant's claim 10, as amended, now recites "...A transparent port for a high rate network comprising ... a programmable link instigation PLI for reporting a set of performance parameters for a data signal of an arbitrary rate R1' ... a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said data signal and configuring said PLI according to said first protocol ... and ... a transmitter unit connected to said PLI for launching an outgoing signal of said first protocol, comprising user information within said data signal; and *a reverse mapping unit for rearranging bits of a container signal of a second protocol into said data signal of said first protocol...*"

Accordingly, Applicant has amended claim 10 to include subject matter indicated as allowable by the Examiner. For at least this reason, claim 10 and associated dependent claims 11-17 are patentably distinct over the combination of Miller and Hershey, and the rejection should be withdrawn.

New Claims 23-33

Applicant has added new claims 23-33, which incorporate limitations previously indicated as allowable by the Examiner into parent claim 10. Accordingly, for at least this reason, claims 23-33 are patentably distinct over the combination of references, and the rejection should be withdrawn.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Lindsay McGuinness, Applicants' Attorney at 978-264-6664 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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MARKED-UP CLAIMS

1. (original) A transparent port for a high rate network comprising:

a receiver unit for receiving an incoming signal of an arbitrary data rate R1 and extracting a user signal and a data clock;

a programmable link termination PLT for reporting a set of performance parameters for said incoming signal; and

a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said incoming signal and configuring said PLT according to said first protocol.

2. (original) A transparent port as claimed in claim 1, wherein said PLT translates said user signal into a data signal whenever said rate R1 corresponds to a provisioned first protocol and passes said user signal unchanged whenever said rate R1 is not recognized by said processing unit.

3. (original) A transparent port as claimed in claim 1, wherein said PLT performs one or more of a framing, an error count, a code conversion, and a parity correction operation.

4. (original) A transparent port as claimed in claim 2, further comprising a mapping unit for rearranging the bits of said data signal into a container signal of a rate R corresponding to a second protocol.

5. (original) A transparent port as claimed in claim 1, wherein said PLT comprises logic gates configured to perform measurement of a provisioned parameter.

6. (original) A transparent port as claimed in claim 1, wherein said PLT is a programmable gate array.

7. (original) A transparent port as claimed in claim 1, wherein said set of performance parameters includes a previous section fail indicator.

8. (original) A transparent port as claimed in claim 1, wherein said set of performance parameters includes one or more of signal strength, clock continuity and jitter.

9. (original) A transparent port as claimed in claim 1, wherein said PLT performs one ore more of a framing, an error count, a code conversion, and a parity correction operation.

10. (Currently Amended) A transparent port for a high rate network comprising:

a programmable link instigation PLI for reporting a set of performance parameters for a data signal of an arbitrary rate R1';

a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said data signal and configuring said PLI according to said first protocol; ~~and~~

a transmitter unit connected to said PLI for launching an outgoing signal of said first protocol, comprising user information within said data signal; and

a reverse mapping unit for rearranging the bits of a container signal of a second protocol into said data signal of said first protocol.

11. (original) A transparent port as claimed in claim 10, wherein said PLI translates said data signal into a user signal whenever said rate R1' corresponds to a provisional first protocol, and passes said data signal unchanged whenever said rate R1 is not recognized by said processing unit.

12. (Cancelled).

13. (original) A transparent port as claimed in claim 10, wherein said PLI comprises logic gates configured to perform measurement of a provisioned parameter.

14. (original) A transparent port as claimed in claim 10, wherein said PLI is a programmable gate array.

15. (original) A transparent port as claimed in claim 10, wherein said set of performance parameters includes a previous section fail indicator.

16. (original) A transparent port as claimed in claim 10, wherein said set of performance parameters includes signal strength, clock continuity and jitter.

17. (original) A transparent port as claimed in claim 10, wherein said PLI performs one or more of a framing, an error count, a code conversion, and a parity correction operation.

18. (original) A method for transmitting a continuous digital signal of an arbitrary rate R1 over a synchronous network as a transparent tributary, comprising:

at a transmit terminal, selecting a container signal of a rate R, higher than said rate R1;

detecting the rate R1 of said continuous digital signal and determining a first protocol corresponding to said rate R1;

measuring according to a first protocol a set of performance parameters on said continuous signal and reporting said set of performance parameters; and

translating said set of performance parameters from said first protocol to a second protocol characterizing said container signal and providing said translated set into said container signal.

19. (original) A method as claimed in claim 18, further comprising transmitting said container signal from said transmit terminal to a receive terminal.

20. (original) A method as claimed in claim 18, further comprising informing said receive terminal of said rate R1 and of said first protocol through signaling.

21. (original) A method as claimed in claim 20, further comprising:

at the receive terminal, recovering said container signal;

extracting said set of performance parameters from said container signal; and

reconstituting said continuous signal based on said rate R1.

22. (original) A method as claimed in claim 21, further comprising transmitting said continuous signal with said set of performance parameter to a user.

23. (New) A transparent port for a high rate network comprising:

a programmable link instigation PLI for reporting a set of performance parameters for a data signal of an arbitrary rate R1';

a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said data signal and configuring said PLI according to said first protocol;

a transmitter unit connected to said PLI for launching an outgoing signal of said first protocol, comprising user information within said data signal; wherein said PLI translates said data signal into a user signal whenever said rate R1' corresponds to a provisional first protocol, and passes said data signal unchanged whenever said rate R1 is not recognized by said processing unit.

24. (New) A transparent port as claimed in claim 23, wherein said PLI comprises logic gates configured to perform measurement of a provisioned parameter.

25. (New) A transparent port as claimed in claim 23, wherein said PLI is a programmable gate array.

26. (New) A transparent port as claimed in claim 23, wherein said set of performance parameters includes a previous section fail indicator.

27. (New) A transparent port as claimed in claim 23, wherein said set of performance parameters includes signal strength, clock continuity and jitter.

28. (New) A transparent port as claimed in claim 23, wherein said PLI performs one or more of a framing, an error count, a code conversion, and a parity correction operation.

29. (New) A transparent port for a high rate network comprising:

a programmable link instigation PLI for reporting a set of performance parameters for a data signal of an arbitrary rate R1', wherein said set of performance parameters includes a previous section fail indicator;

a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said data signal and configuring said PLI according to said first protocol; and

a transmitter unit connected to said PLI for launching an outgoing signal of said first protocol, comprising user information within said data signal.

30. (New) A transparent port as claimed in claim 29, wherein said PLI comprises logic gates configured to perform measurement of a provisioned parameter.

31. (New) A transparent port as claimed in claim 29, wherein said PLI is a programmable gate array.

32. (New) A transparent port as claimed in claim 29, wherein said PLI performs one or more of a framing, an error count, a code conversion, and a parity correction operation.

33. (New) A transparent port as claimed in claim 23, wherein said set of performance parameters includes a previous section fail indicator.